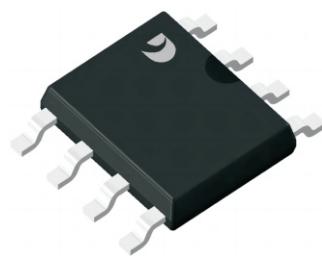




23A 30V N-channel enhanced MOSFET

SOP-8



ROHS
COMPLIANT

Description

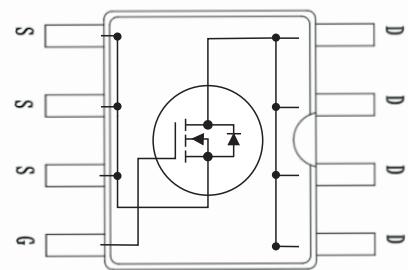
This N-Channel specified MOSFET is a ruggedized version of Fairchild's Semiconductor's advancedPowerTrench process. It has been optimized for powermanagement applications with a wide range of gatedrive voltage

Features

- $R_{DS(ON)} < 6.0\text{m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=20\text{A}$
- Optimized for use in battery circuit applications
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile SOP-8 package

Mechanical data

- Case: SOP-8
- RoHS compliant
- Case Material: "Green" molding compound, UL flammability classification 94V-0, "Halogen-free".



Absolute Maximum Ratings ($T_a=25^\circ\text{C}$, Unless Otherwise Specified)

Parameter	Symbols	Ratings	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_a=25^\circ\text{C}$	I_D	23	A
Pulsed Drain Current $T_a=25^\circ\text{C}$	I_{DM}	69	A
Power dissipation $T_a=25^\circ\text{C}$	P_{tot}	3.1	W
Operating junction and storage temperature	T_j, T_{stg}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbols	Ratings	Units
Device on PCB cooling area (Note1)	R_{thJA}	80	$^\circ\text{C}/\text{W}$

NOTE:

1.Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR-4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.



Electrical Characteristics (TA=25°C, Unless Otherwise Specified)

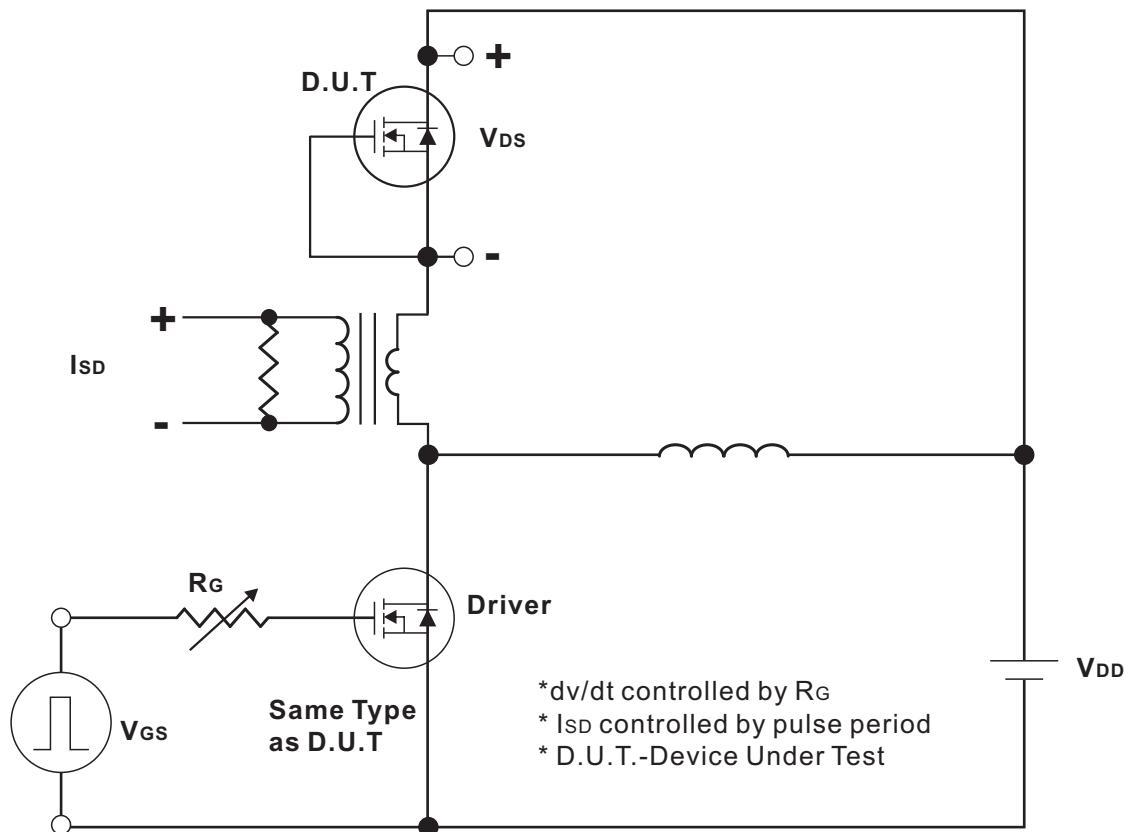
Parameter	Symbols	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=20A$ $V_{GS}=4.5V, I_D=15A$		4.7 8.0	6.0 10.0	$m\Omega$
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=25V,$ $V_{GS}=0V,$ $f=1.0MHz$		1769		pF
Output Capacitance	C_{oss}			200		pF
Reverse Transfer Capacitance	C_{rss}			167		pF
Gate resistance	R_G	$V_{DS}=0V, FREQ=1.00MHz$		3.3		Ω
Switching Characteristics						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=15V, V_{GS}=4.5V,$ $I_D=20A(NOTE1,2)$		32		nC
Gate-Source Charge	Q_{GS}			13		nC
Gate-Drain Charge	Q_{GD}			13		nC
Turn-On Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=15V, V_{GS}=10V,$ $R_G=6\Omega, I_D=20A$ $R_L=0.8\Omega$ (NOTE1,2)		13		ns
Turn-On Rise Time	t_R			15		ns
Turn-Off Delay Time	$t_{D(OFF)}$			75		ns
Turn-Off Fall Time	t_F			25		ns
Drain-source Diode Characteristics And Maximum Ratings						
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_{SD}=2.5A, V_{GS}=0V$			1.2	V
Diode continuous forward current	I_S				23	A
Reverse Recovery time	trr	$I_F=20A$ $di/dt=100A/us$		11		nS
Reverse Recovery Charge	Qrr			1.6		nC

Notes:

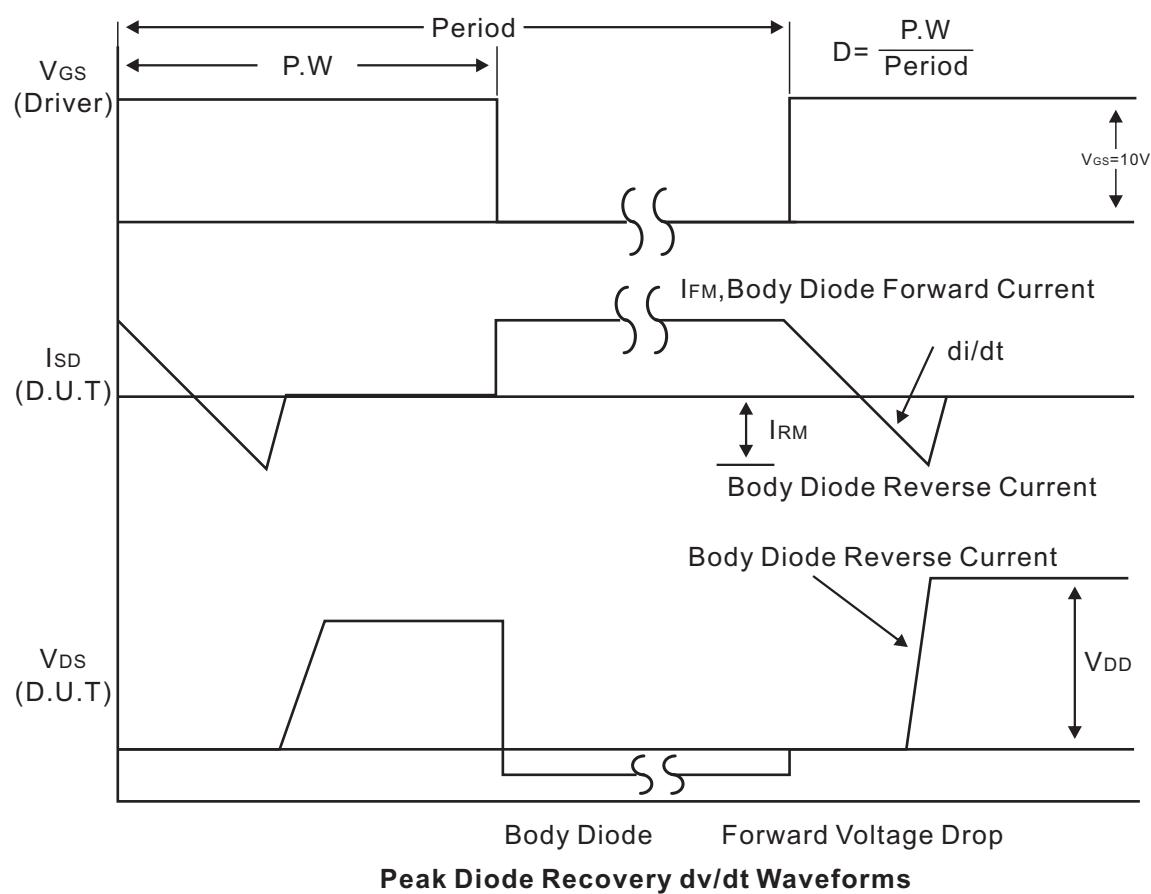
1. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature.



Test Circuits and waveforms

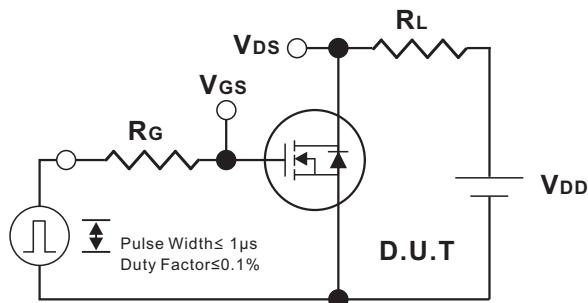


Peak Diode Recovery dv/dt Test Circuit

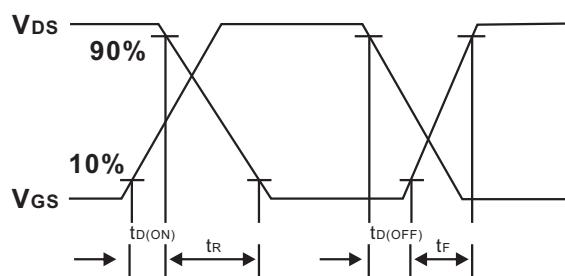




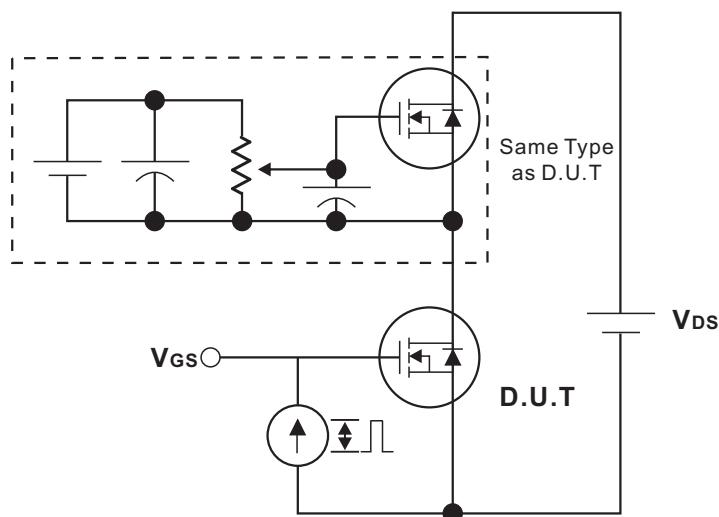
Test Circuits and waveforms



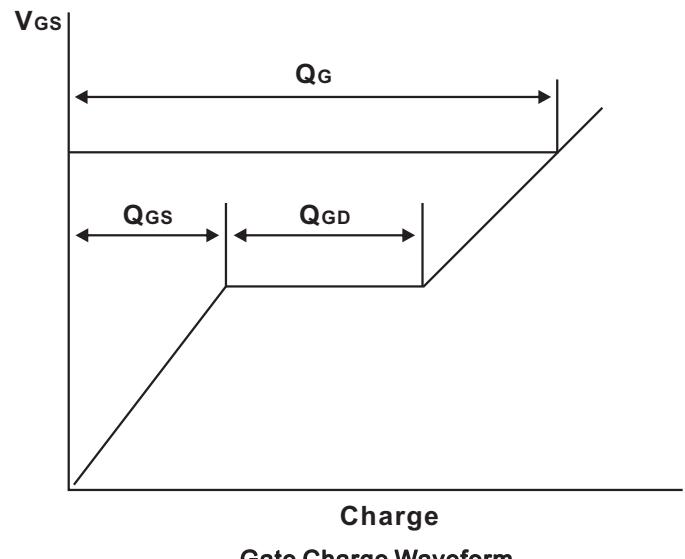
Switching Test Circuit



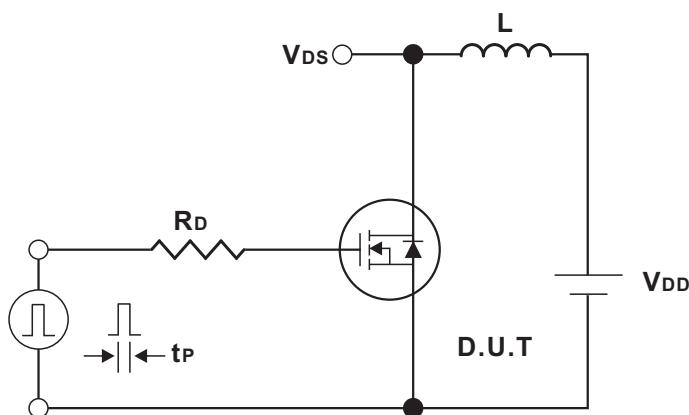
Switching Waveforms



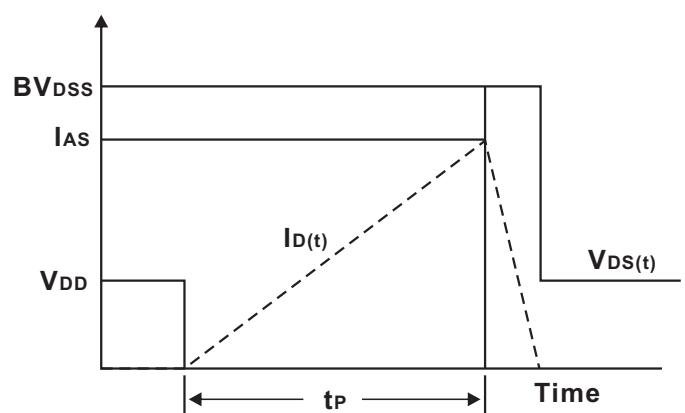
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms



Typical Characteristics

Fig.1 Output characteristics

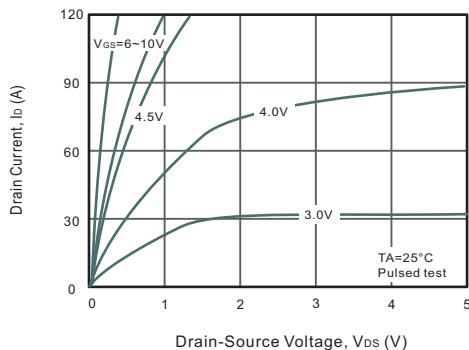


Fig.2 Power Dissipation

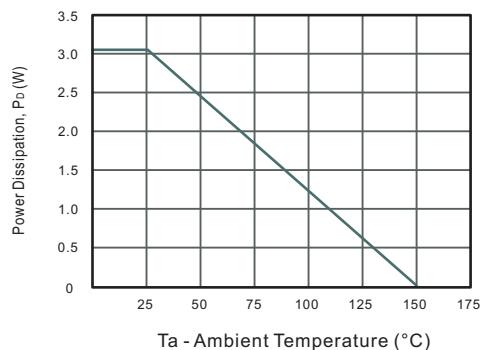


Fig.3 Drain Current Derating

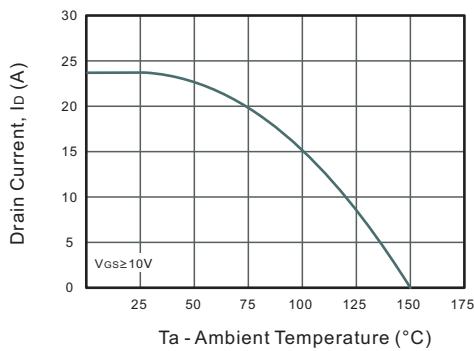


Fig.4 Drain-Source On-Resistance vs. Drain Current

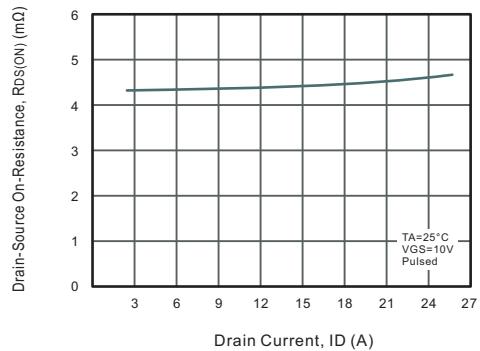


Fig.5 Gate Threshold Voltage vs. Junction Temperature

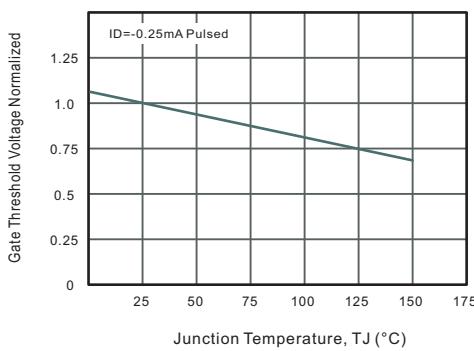


Fig.6 Body-diode Forward Characteristics

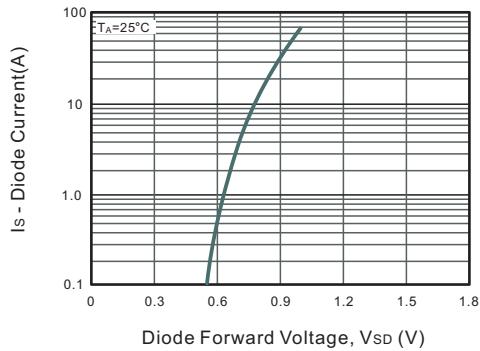


Fig.7 Drain-Source On-Resistance vs. Junction Temperature

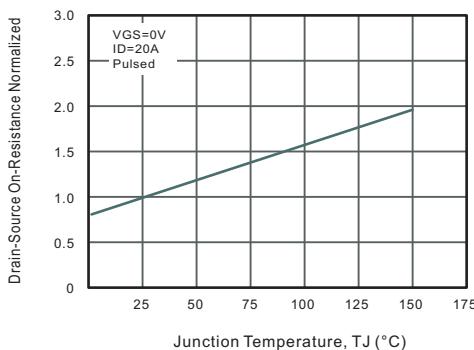
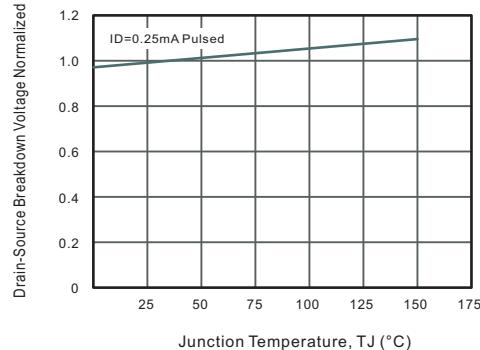


Fig.8 Breakdown Voltage vs. Junction Temperature





Typical Characteristics

Fig.9 Capacitance Characteristics

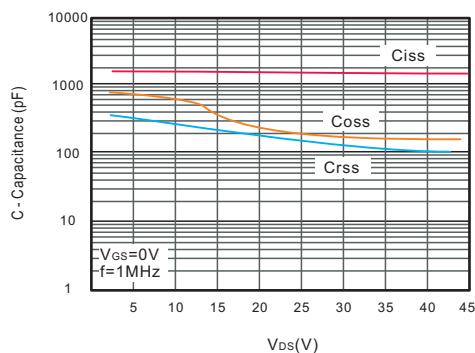


Fig.10 Gate Charge Characteristics

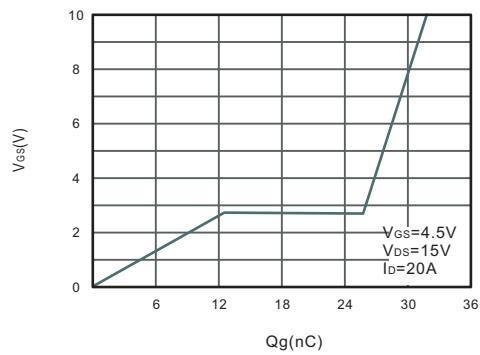


Fig.11 Safe Operating Area

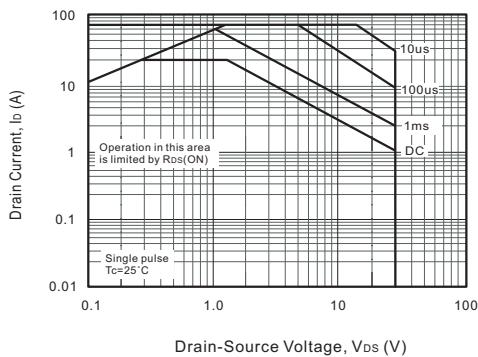
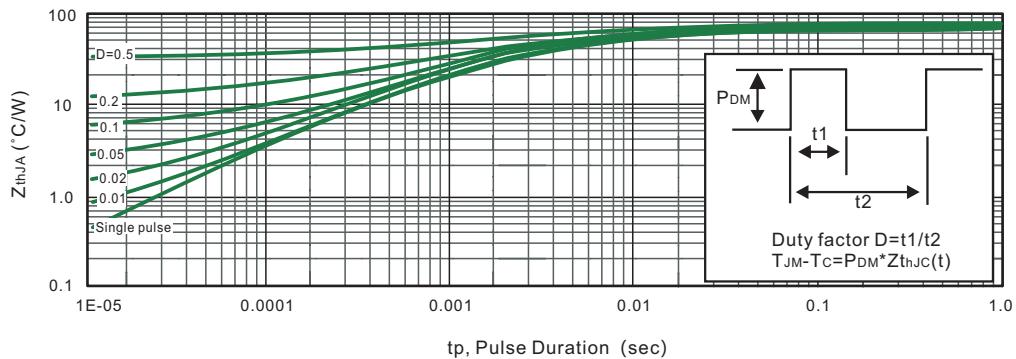
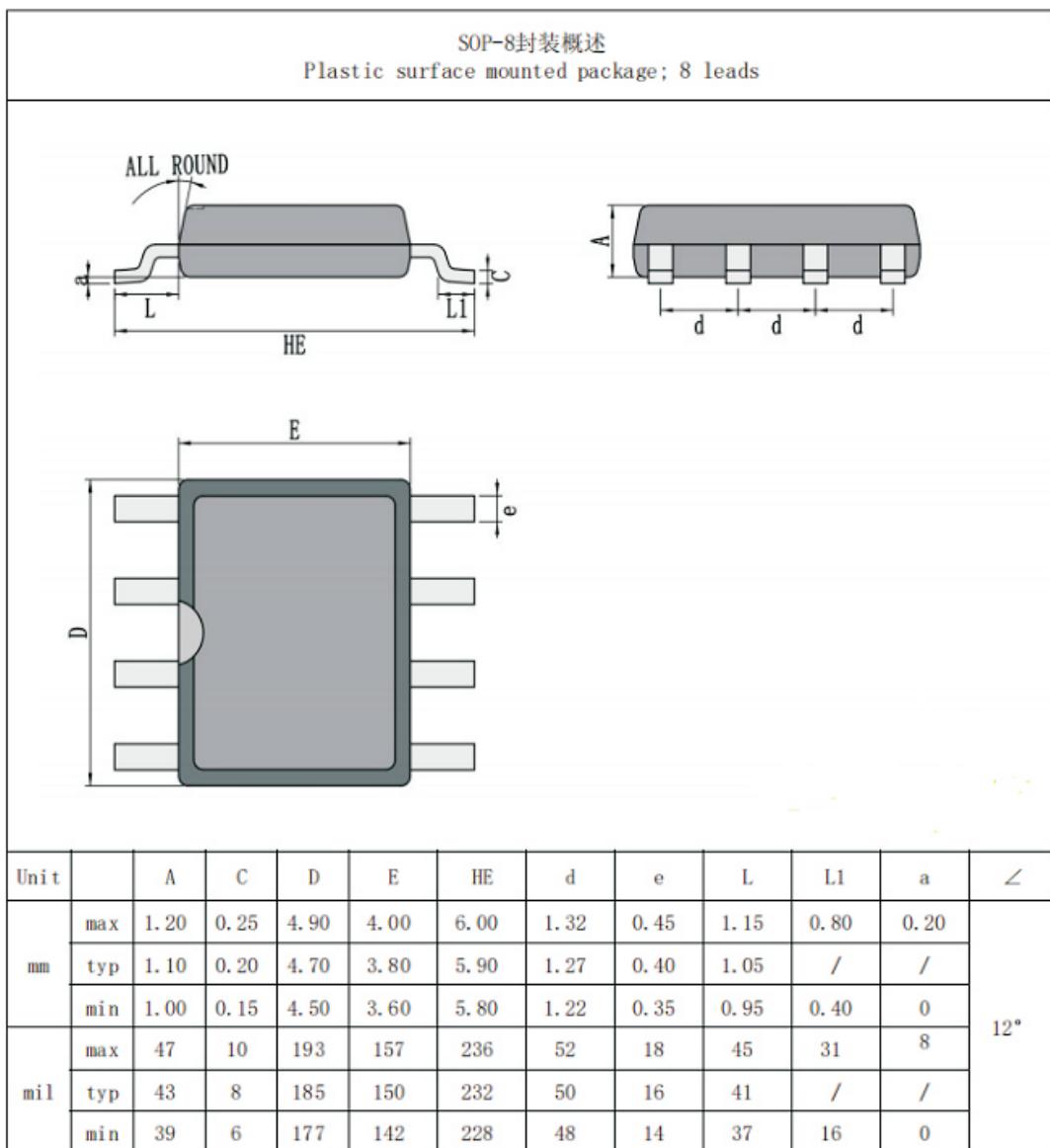


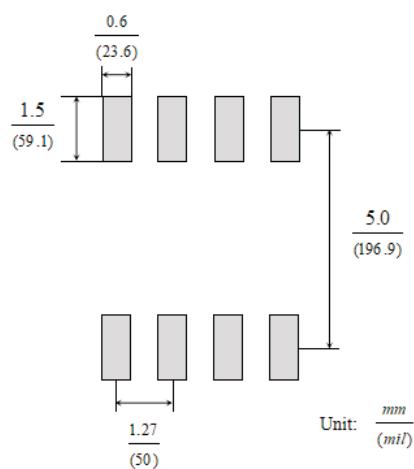
Fig.12 Max. Transient Thermal Impedance





Marking

Type number	Marking code
S4R7N30XR8	S4R7N30XR8



SUGGESTED SOLDER PAD LAYOUT



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